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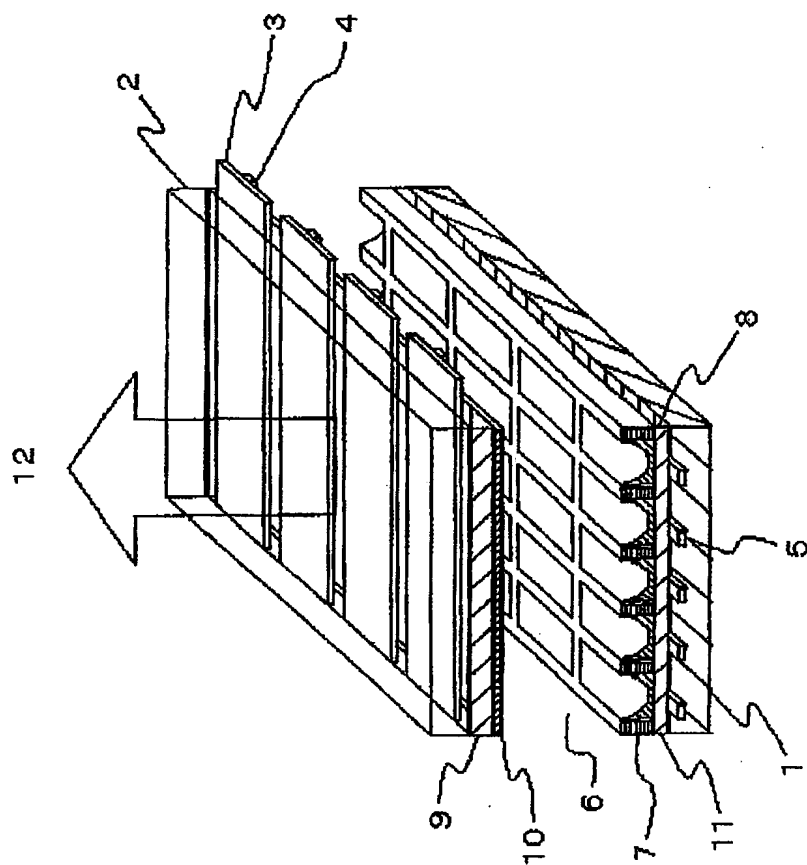
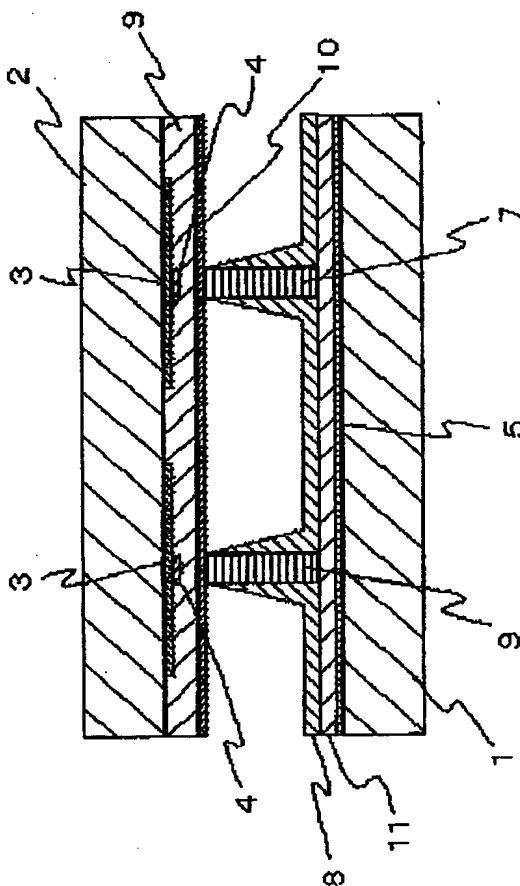


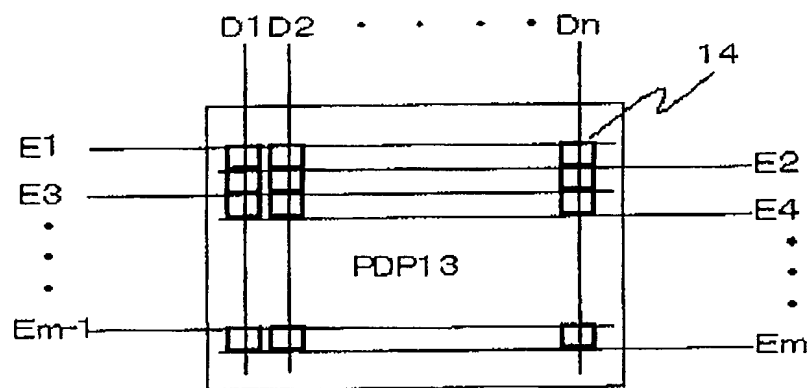
FIG. 1 PRIOR ART

FIG.2
PRIOR ART



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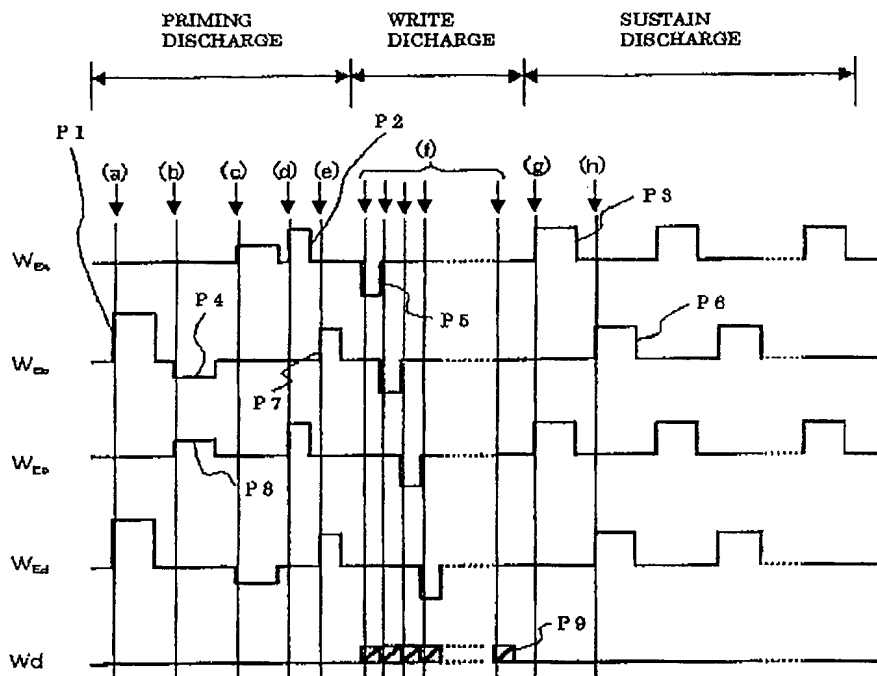
FIG.3
PRIOR ART



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FIG. 4
 PRIOR ART



- P1 : PRIMING DISCHARGE PULSE P_{p1}
 P2 : PRIMING DISCHARGE ELIMINATION PULSE P_{pe}
 P3 : SUSTAIN PULSE
 P4 : PRIMING DISCHARGE PULSE P_{p2}
 P5 : SCAN PULSE
 P6 : SUSTAIN PULSE
 P7 : PRIMING DISCHARGE ELIMINATION PULSE P_{pe}
 P8 : PRIMING DISCHARGE PULSE P_{p3}
 P9 : DATA PULSE

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FIG.5A
 PRIOR ART

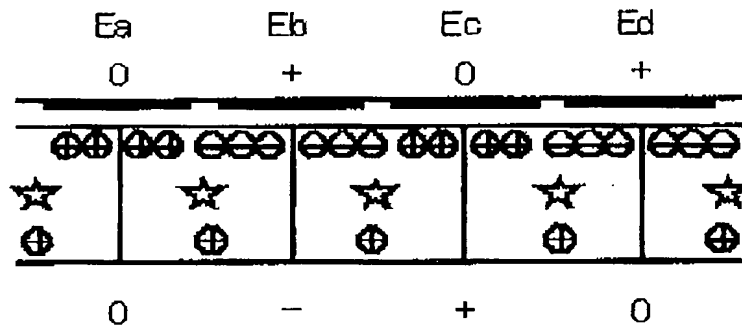


FIG.5B
 PRIOR ART

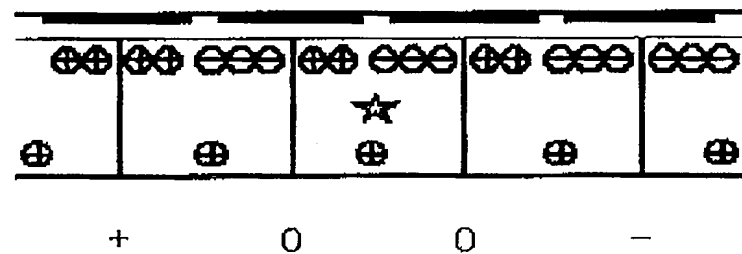


FIG.5C
 PRIOR ART

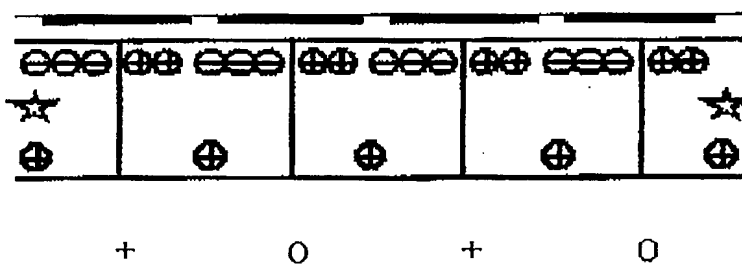


FIG.5D
 PRIOR ART

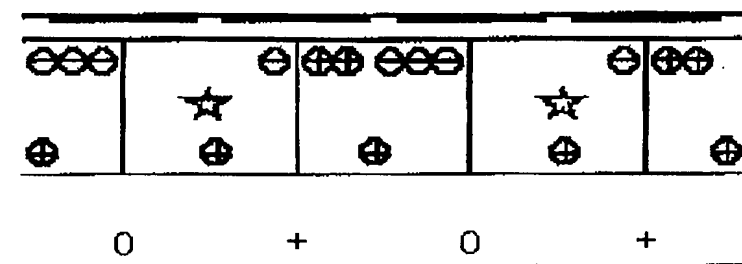
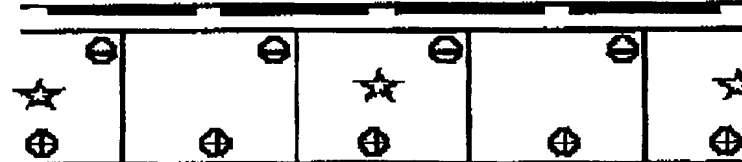


FIG.5E
 PRIOR ART



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FIG.5F
 PRIOR ART

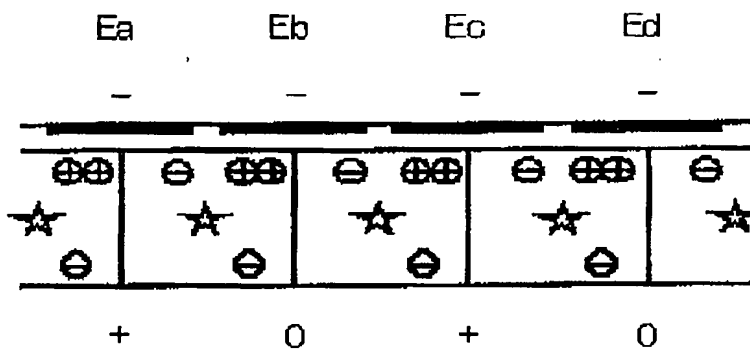


FIG.5G
 PRIOR ART

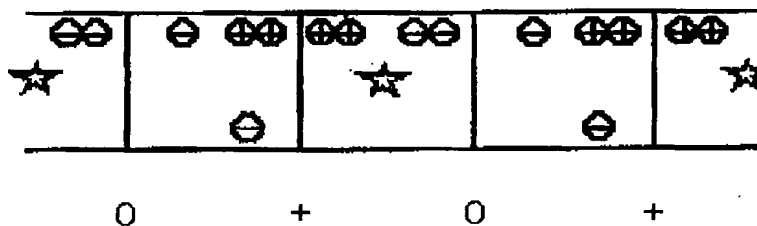


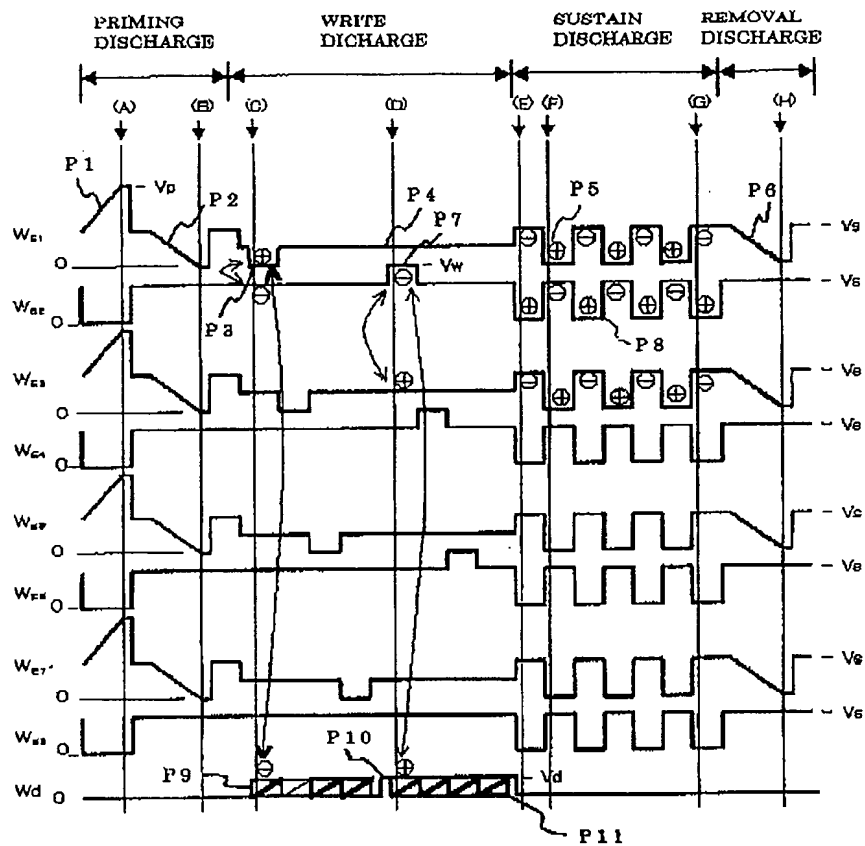
FIG.5H
 PRIOR ART



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FIG.6



- P1 : PRIMING DISCHARGE PULSE
- P2 : PRIMING DISCHARGE REMOVAL PULSE
- P3 : SCAN PULSE
- P4 : SCAN BASE PULSE
- P5 : SUSTAIN PULSE
- P6 : SUSTAIN REMOVAL PULSE
- P7 : SCAN PULSE
- P8 : SUSTAIN PULSE
- P9 : DATA PULSE
- P10 : DATA BASE PULSE
- P11 : DATA PULSE

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FIG. 7A

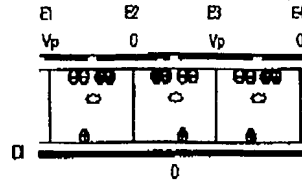


FIG. 7B

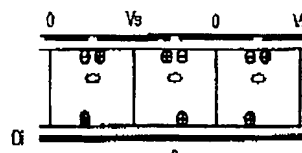


FIG. 7C

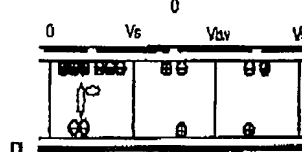


FIG. 7D

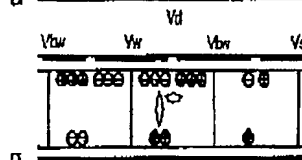


FIG. 7E

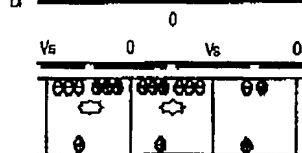


FIG. 7F

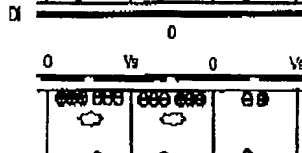


FIG. 7G

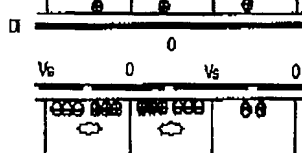
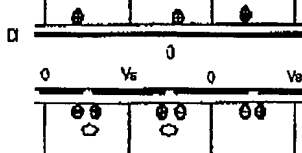


FIG. 7H



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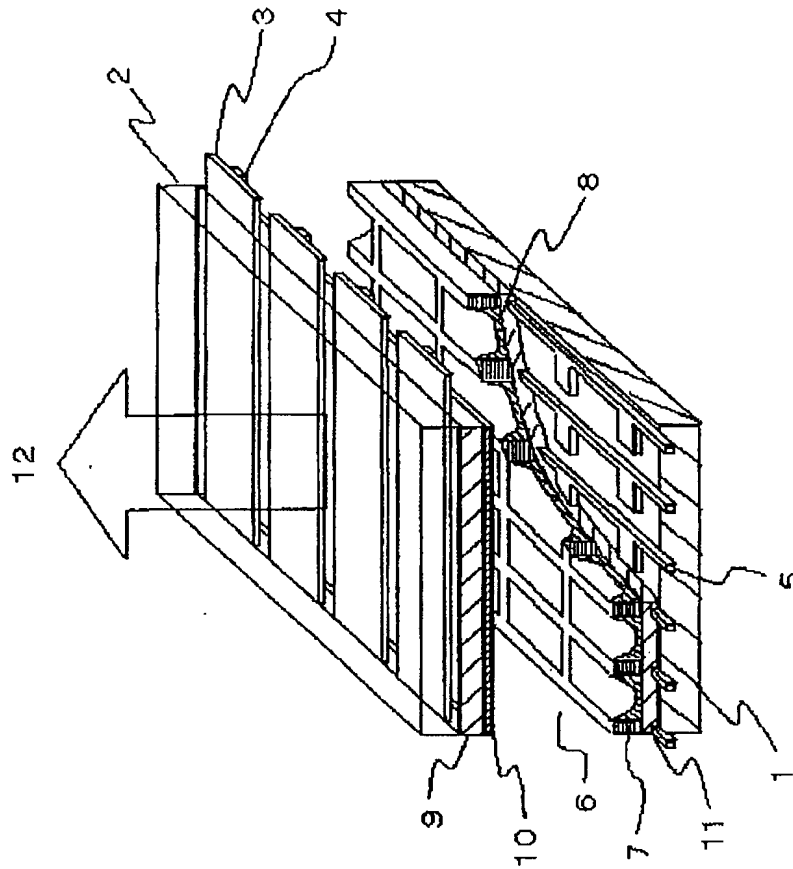
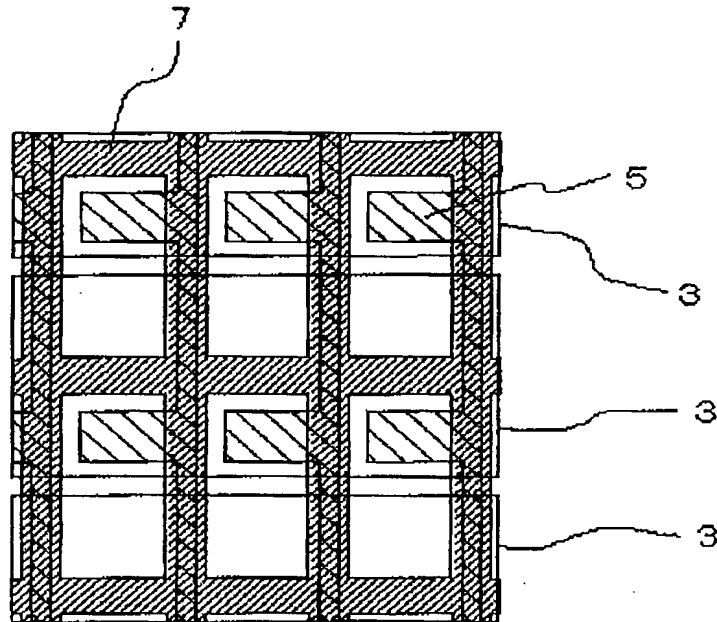


FIG. 8

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FIG. 9



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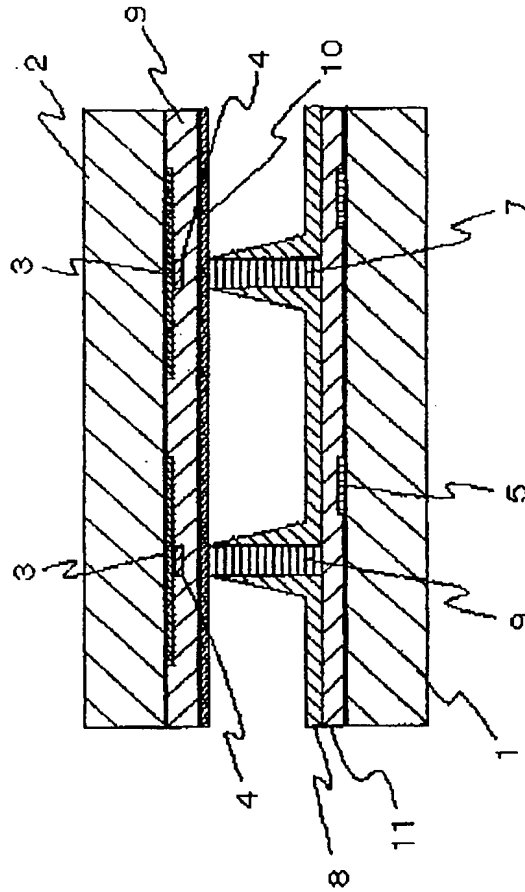


FIG.10

FIG. 10

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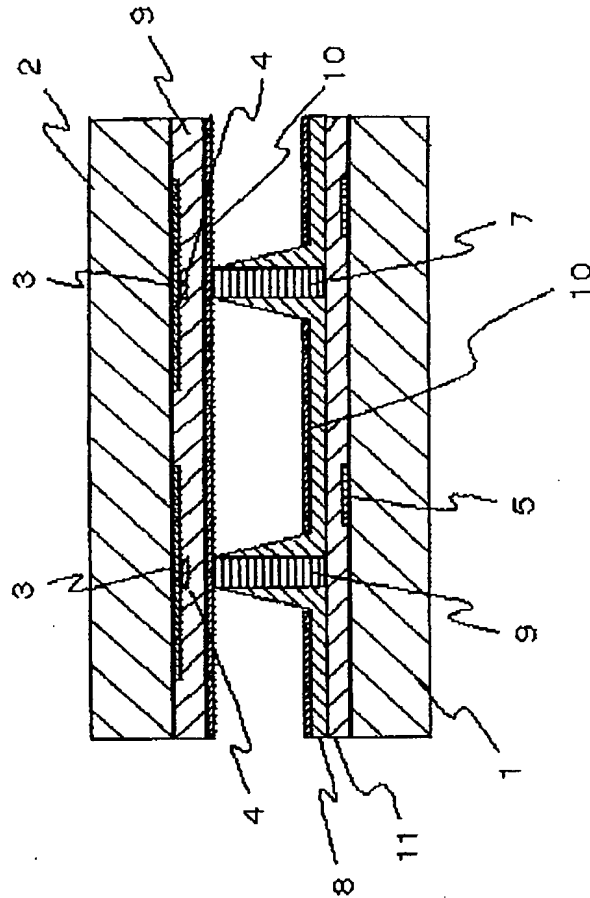


FIG.11

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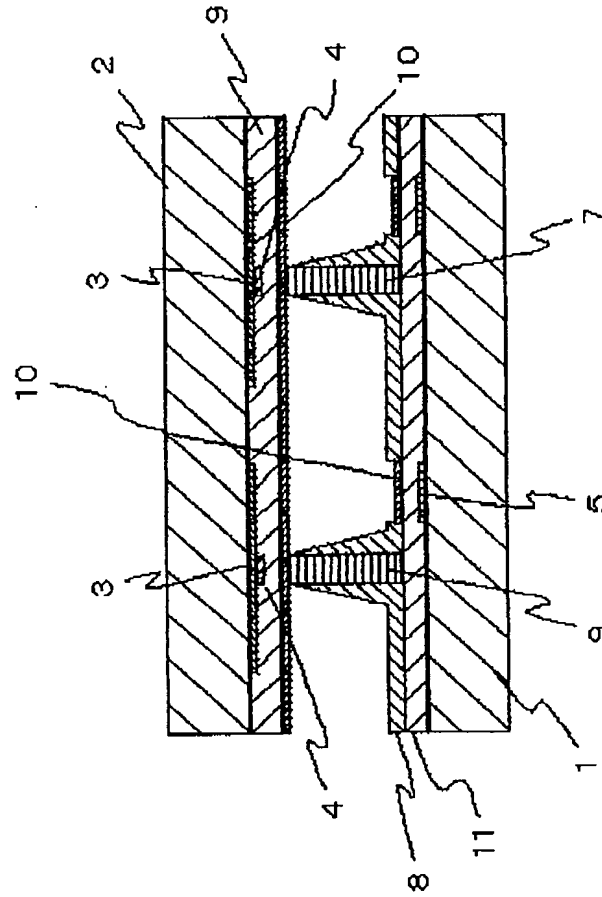
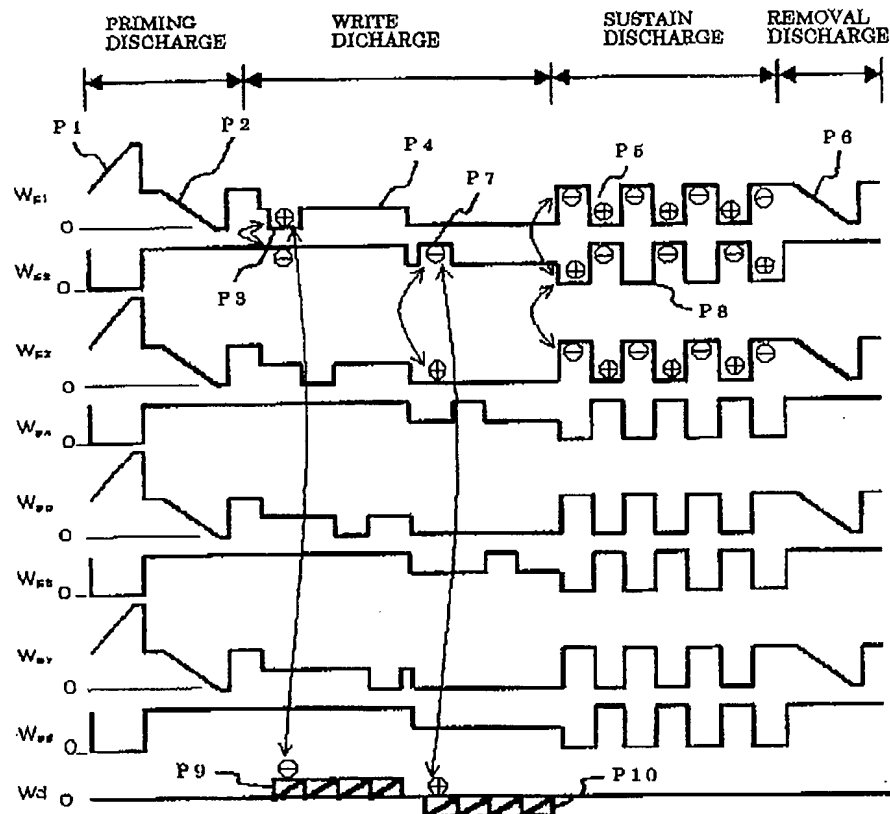


FIG.12

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FIG.13

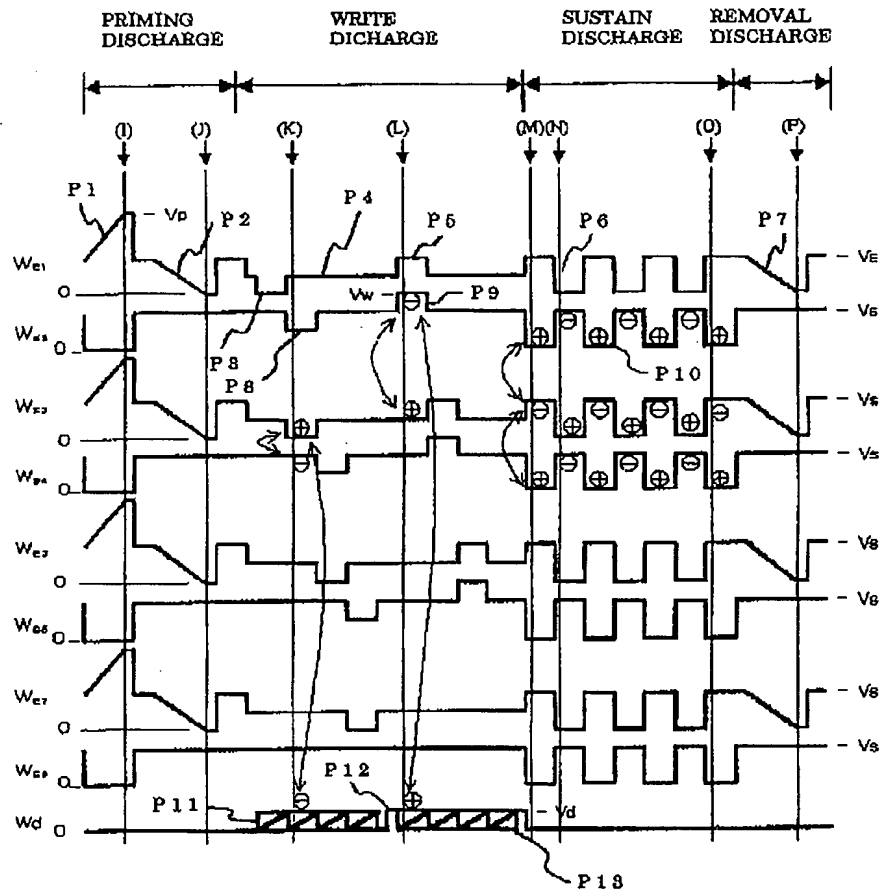


- P1 : PRIMING DISCHARGE PULSE
- P2 : PRIMING DISCHARGE REMOVAL PULSE
- P3 : SCAN PULSE
- P4 : SCAN BASE PULSE
- P5 : SUSTAIN PULSE
- P6 : SUSTAIN REMOVAL PULSE
- P7 : SCAN PULSE
- P8 : SUSTAIN PULSE
- P9 : DATA PULSE
- P10 : DATA PULSE

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FIG.14



- P1 : PRIMING DISCHARGE PULSE
- P2 : PRIMING DISCHARGE REMOVAL PULSE
- P3 : SCAN PULSE
- P4 : SCAN BASE PULSE
- P5 : WRITE CANCEL PULSE
- P6 : SUSTAIN PULSE
- P7 : SUSTAIN REMOVAL PULSE
- P8 : WRITE CANCEL PULSE
- P9 : SCAN PULSE
- P10 : SUSTAIN PULSE
- P11 : DATA PULSE
- P12 : DATE BASE PULSE
- P13 : DATA PULSE

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Figure 1 shows a schematic diagram of the experimental setup. A horizontal tube is divided into four sections labeled E1, E2, E3, and E4. E1 and E3 contain a gas phase (Vp) and a liquid phase (0). E2 and E4 contain only a liquid phase (0). The tube is connected to a reservoir at the bottom. Arrows indicate the flow of gas and liquid phases.

The diagram shows a four-stage shift register with stages labeled V_s , V_w , V_{bw} , and V_s . Each stage contains a row of four circles representing bits. In the first V_s stage, the top row has two 1s and two 0s, and the bottom row has two 0s and two 1s. In the V_w stage, the top row has four 1s and the bottom row has two 1s and two 0s. In the V_{bw} stage, the top row has four 1s and the bottom row has two 1s and two 0s. In the final V_s stage, the top row has four 1s and the bottom row has two 1s and two 0s. Arrows indicate the shift of bits from left to right between stages. Below the register, a 'Di' input is shown with a '0' value.

0